San Diego, CA, May 28, 2015 - Speakers at the 5G Forum hosted by the Center for Wireless Communications (CWC) at UC San Diego discussed the various directions that 5G technology is headed towards. These included a future in mobile and remote health care, smart cities, and increased mobile connectivity.

“Ultimately, we see a world where there’s wireless gigabit [connectivity] everywhere,” said Khurram Sheikh, President of SiBEAM, which he dubbed “the gigabit wireless everywhere company.”

Sheikh presented SiBEAM’s Snap Technology, which is designed to replace USB connectors on various devices including smartphones, computers, tablets, and cameras. Uses for SiBEAM Snap wireless connectors were described as “sync and run” or “sync and play.” With Snap Technology, a smartphone can be placed next to a laptop and transfer content without a physical USB connection.

Another vision for 5G is faster data rates. Greg VanWiggeren, Department Manager at Keysight Technologies, said that to achieve data rates that are up to one hundred times faster than those of today, technologies must start utilizing spectra in the millimeter wave bands. VanWiggeren discussed how recent efforts at Keysight Technologies focus on better understanding millimeter wave channels and how to incorporate them in 5G.

Gabriel Rebeiz, professor of Electrical and Computer Engineering (ECE) at UC San Diego, presented his work on phased arrays for 5G systems. A recent collaborative effort between Rebeiz and TowerJazz, featured in Semiconductor Today and CNN Money, demonstrated the first 256-element (16 × 16) silicon wafer-scale phased array transmitter with integrated high-efficiency antennas operating in the 56–65 GHz frequency range.

Rebeiz noted that this is the largest RF chip ever built in the world. This work also demonstrates that the integration of the antennas and phased arrays on the same chip is important for high-performance wireless communications.

“Our vision that we’ve had for a long time is more integration,” said Rebeiz.

Ian Galton, ECE professor at UC San Diego, noted that in order to continue on the path to 5G, the technology will need new analog circuit blocks that are more digital-like than conventional analog circuitry and use extensive digital calibration to achieve high performance. Galton’s lab built such a chip that achieves state-of-the-art analog to digital converter (ADC) performance with much lower area than the closest competing ADC. Galton also described that without such techniques, high performance analog blocks are prohibitively difficult to achieve in sub-20 nm CMOS.

Galton also pointed out that the CMOC IC technology scaling phenomenon that has come to be known as Moore’s Law has made each new mobile communications generation, including 5G, possible.

“We’re pretty much at the end of Moore’s Law [so] my personal belief is that there won’t be a 6G,” added Galton.

The forum also focused on the power challenges that researchers in 5G technologies need to consider in their work. According to Sujit Dey, ECE professor at UC San Diego and director of CWC, the mobile networks will leave behind a much larger carbon footprint than the wired networks. As technology evolves towards 5G, researchers must also look into ways to save power while still achieving high performance in next-generation devices and connections.
“The overall consensus is about 50 to 60 percent of the energy is being consumed by the base stations,” said Dey.

On the other hand, demanding applications like video are draining the mobile device batteries much faster.

“We have been looking at various ways of addressing this problem. I’m going to talk about what kind of data delivery techniques we may come up with in which we can mitigate some of these issues.”

An example that Dey presented was to vary the data delivery rate opportunistically, and even stopping the transmission at certain times, to allow selective shutting off of base station antennas as well as idling of mobile device batteries from time to time.

Another challenge related to power usage is how to mitigate the thermal output of small devices such as phones and tablets. This was the issue that Varada Gopalakrishnan, Senior Principal Engineer at Amazon Lab126, posed to the audience. The performance of today’s devices is not limited by the number of cores or by the amount of processing power available, said Gopalakrishnan. Rather, the performance is limited by the heat they produce.

“Adding more cores is not the answer we need to solve,” said Gopalakrishnan, because more cores would consume more power, produce more heat, and ultimately inhibit performance.

Joseph Soriaga, Senior Staff and Manager of R&D at Qualcomm, mentioned that a way to get to lower power is through lower latency. “At the device level, it [lower latency] is actually very important...if we shorten the timeline, we don’t have to buffer as much. We can shut the radio off and shut the baseband off sooner. That actually can make for a more energy-efficient design leveraging the wider bandwidth that we’re getting,” said Soriaga.

Ultra-low power was also a topic of discussion. Patrick Mercier, Assistant Professor of ECE at UC San Diego, shared some of his recent research efforts on harvesting 1 nanowatt of power from the inner ear of guinea pigs. Mercier described how this type of power, although very low, can be harvested and buffered over time until it can be used for applications that require low data rates, such as glucose sensing.

Mercier also stressed how this research can enable new opportunities.

“We can start to explore different forms of energy harvesting that people perhaps have previously not considered due to their low available powers.”