A Battery-Connected Symmetric Modified Multilevel Ladder Converter Achieving 0.45W/mm^2 Power Density and 90% Peak Efficiency

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***Abstract*—A symmetric modified multilevel ladder (SMML) DC-DC converter is presented which relaxes the trade-off between efficiency and power density by employing an inherent phase interleaving between the SC phases and by reducing the current ripple in the inductor, both allowing for reduced conduction losses. In addition, the SMML topology minimizes or eliminates the circuit overhead required in conventional multilevel converters to generate extra supply rails for the drivers and to balance the flying capacitors, allowing the converter to be solely powered by a Li-ion battery. A prototype shows the converter can achieve a power density of 0.45W/mm^2, a peak efficiency of 90%, and can provide conversion ratios up to 15× with efficiency >70%.**

I. Introduction

An increasingly large fraction of the board area in modern mobile devices is occupied by power management integrated circuits (PMICs) and their associated passives. In general, it is difficult for PMICs to achieve high efficiency, which is necessary to extend battery life, while also operating with high power density, which is necessary to minimize occupied area, especially when operating from Li-ion batteries (3.3-to-4.5V) and converting down to 0.3-1V rails as required by modern scaled SoCs (i.e. conversion ratios of 3-15×). To operate from Li-ion voltages, designs employing thin-oxide transistors must resort to transistor stacking to block the large input voltages, which limits efficiency and power density, especially at large conversion ratios [1].

Since stacking is required to block Li-ion voltages using thin-oxide transistors, recent work on hybrid converters [2]–[7] has suggested exploiting the stack to add further functionality - for example by adding flying capacitors within the stack to form a switched-capacitor (SC) network that can provide additional features such as reduced voltage swing across the inductor [4]–[7]. Despite the increased component and switch count of such hybrid converters, the reduced swing across the inductor enables use of physically smaller inductors iso-performance, thereby enabling an efficiency and/or power density advantage. However, most prior-art multilevel converters require auxiliary DC-DC converters to generate the needed supply rails to control and operate the converter, the area and/or power overhead of which is not included [5], [6], while topology-constrained conduction losses through the series resistance of switches/capacitors can in some cases hinder efficiency or power density. Moreover, some switches and capacitors in some SC topologies (e.g., series-parallel) have higher blocking voltage and hence additional stacking might be required. Also, the flying capacitors in most of these topologies require some balancing control loops to maintain network stability.

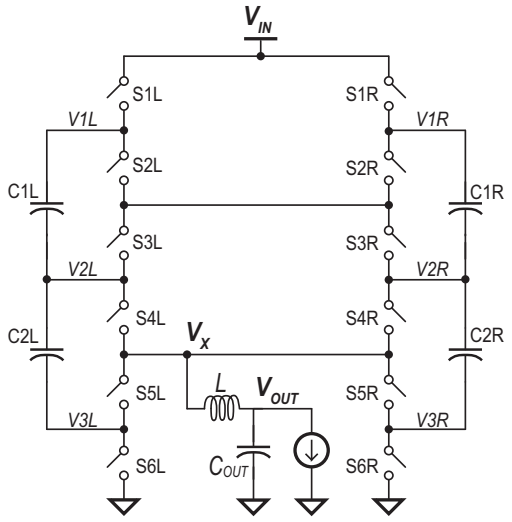

Fig. 1. A symmetric modified multilevel ladder (SMML) DC-DC converter.

To overcome these limitations, this paper presents a Symmetric Modified Multilevel Ladder (SMML) DC-DC converter, shown in Fig. 1, that achieves state-of-the-art power density and high efficiency while operating at Li-ion-to-SoC conversion ratios between 4 and 15×. This topology captures the main advantages of multilevel converters while also providing some additional features: 1) reduced conduction losses in the SC network through an inherent mutli-phase operation where the current is supplied from both supply rails to the output through multiple parallel paths that reduce the effective on-resistance of the switches; 2) naturally-balance flying capacitors without explicit voltage correction circuits; 3) minimum voltage stress across all switches and capacitors, eliminating the need for additional stacking; 4) mitigated internal charge sharing losses between the flying capacitors through a dead-time control technique; 5) inherent inclusion of all power supplies required for the drivers and control circuits, eliminating the need for dedicated power rails.

II. Symmetric Modified Multilevel Ladder Converter Topology and Operation

The SMML converter, shown in Fig. 1, is built upon a modified 3:1 SC ladder topology that consists of four capacitors and 12 switches, the output of which is connected to an inductive low-pass-filter to construct a hybrid topology. The inductor of the low-pass-filter allows for soft charging between the flying capacitors and the output capacitor and hence eliminates the main charge sharing loss existent in conventional SC converters.

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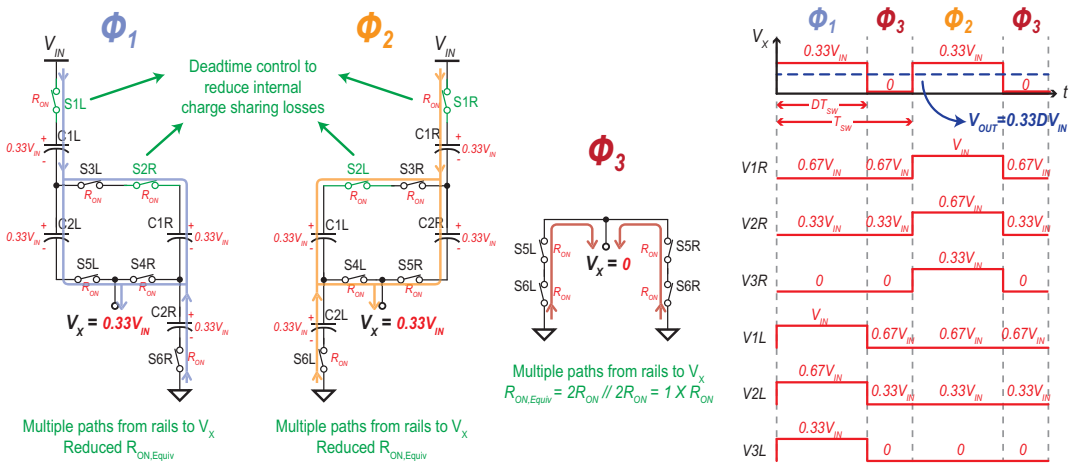

Fig. 2. Illustration of the operating phases of the SMML converter showing the waveforms of the main switching node (V_X) and the internal switching nodes.

Figure 2 shows the switching phases of the SMML converter along with the waveforms of the internal switching nodes. Two phases of the SC network (ϕ_1 and ϕ_2) are used to generate $0.33V_{IN}$ at the switching node V_X, where the flying capacitors are involved in the charge transfer process. A third phase of the SC network (ϕ_3) is used to generate a zero voltage level at the V_X node by directly connecting it to ground while the flying capacitors are kept idle. The circuit is configured so that V_X switches periodically between $0.33V_{IN}$ and 0 by having ϕ_1 followed by ϕ_3, then ϕ_2 followed by another ϕ_3. Since V_X is switching between $0.33V_{IN}$ and 0 instead of V_{IN} and 0 as in a conventional buck converter, the current ripple in the inductor is reduced by at least 1/3, allowing for smaller inductors and/or higher efficiency, while also enabling the SMML converter to operate at high conversion ratios with more relaxed duty cycles compared to a conventional buck converters. Note that the SMML converter implemented in this work operates in the lowest region where V_X switches between $0.33V_{IN}$ and 0. Operating at other regions (e.g., V_X is switching between $0.67V_{IN}$ and $0.33V_{IN}$ or between V_{IN} and $0.67V_{IN}$) is possible but is not practical for SoC voltages less than or equal to 1V.

The two phases producing the $0.33V_{IN}$ voltage level (i.e. ϕ_1 and ϕ_2) feature an inherent phase-interleaving procedure where the load current is drawn from both the supply rails (i.e. V_{IN} and GND) simultaneously as shown in Fig. 2. In conventional multi-phase-interleaving techniques, multiple instances of the circuit are replicated with phase-shifted control signals. In the SMML converter, the phase interleaving is inherent in the circuit operation without the need for extra devices and without the need for complex control circuit. For example, a regular 3:1 ladder would nominally require 3 capacitors and 6 switches, and thus a conventional two-phase circuit would require 6 capacitors and 12 switches. Here, only 4 capacitors are required, a net reduction of 2. Importantly, the inherent phase-interleaving also helps to reduce the total equivalent on-resistance of the circuit, since the load current is divided through multiple paths throughout the SC network. In ϕ_3, switches S5L, S6L, S5R and S6R are turned on simultaneously resulting in an equivalent on-resistance of one power MOSFET. Hence, this topology features reduced on-resistance throughout all the three phases.

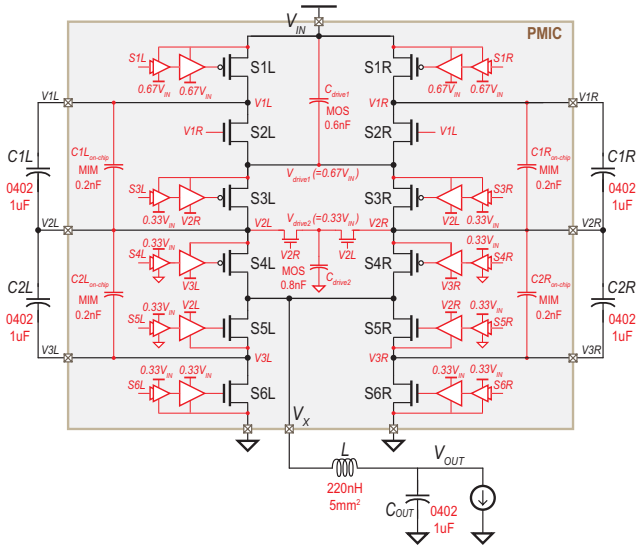

Fig. 3. Full schematic of the implemented SMML converter.

Since the flying capacitors are always stacked between V_{IN} and ground in ϕ_1 and ϕ_2, they are forced to be balanced at $0.33V_{IN}$ naturally without the need for any voltage correction modules. Unfortunately, stacking of the flying capacitors would, without careful control, result in inherent charge sharing losses at the start of each phase due to the voltage imbalance between the capacitors. Fortunately, these charge sharing losses can be mitigated through a careful coarse adjustment of the dead-time between the different control signals of the switches. For example, in the implemented design, switches S2R and S2L are enabled after a brief deadtime-based delay to limit the amount of charge sharing that would otherwise occur between {C2L,C1R} and {C1L,C2R}, respectively, similar to the split-phase control technique in [5], but in this case via deadtime adjustment as opposed to explicit additional phases.

III. Converter Implementation

Figure 3 shows a complete circuit for the proposed SMML converter including all the MOSFET drivers and the internal-rail generation circuits. All of the switches and capacitors

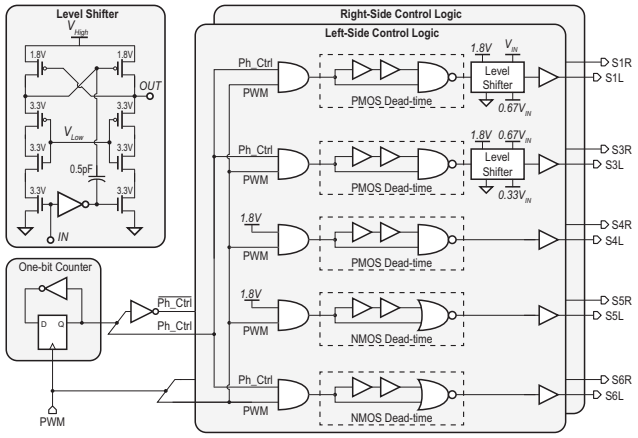

Fig. 4. Generation of the control signals showing level-shifter schematics and dead-time circuits.

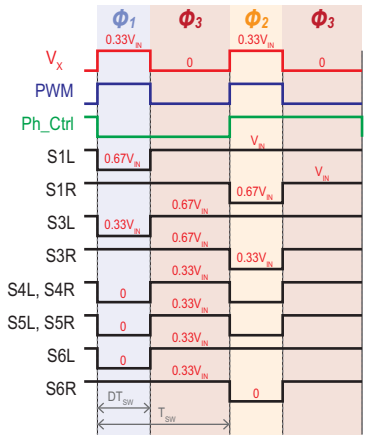

Fig. 5. Timing diagram of the level-shifted control signals of drivers.

experience a maximum voltage stress of $0.33V_{IN}$, which, when using the regular thin-oxide 1.8V transistors in the employed 180nm CMOS technology, results in no additional device stacking required for input voltages up to 4.5V.

A. MOSFET Drivers

All of the drivers of the switches are either driven by the internal switching nodes of the converter (e.g., V1L and V1R), or by a steady-state voltage (e.g., $0.33V_{IN}$ and $0.67V_{IN}$, both of which are also generated internally with minimal circuit overhead), as depicted in Fig. 3; no external power supplies are needed for the drivers. For example, V_{drive1} (=$0.67V_{IN}$) is generated by exploiting the internal node of the converter that is always balanced at $0.67V_{IN}$, and adding a decoupling capacitor (C_{drive1}) to stabilize the node, especially during ϕ_3 when this node is decoupled from the converter switching nodes but is still used by the drivers. Similarly, supply rail V_{drive2} (=$0.33V_{IN}$) is generated using one decoupling capacitor (C_{drive2}) and two small MOSFETs, driven directly by the internal switching nodes V2L and V2R. Small parallel on-chip flying MIM capacitors ($C_{F,on\text{-}chip}$) are used to mitigate the ringing due to wire-bonding parasitic inductance since some of the drivers are powered from the internal switching node of the converter.

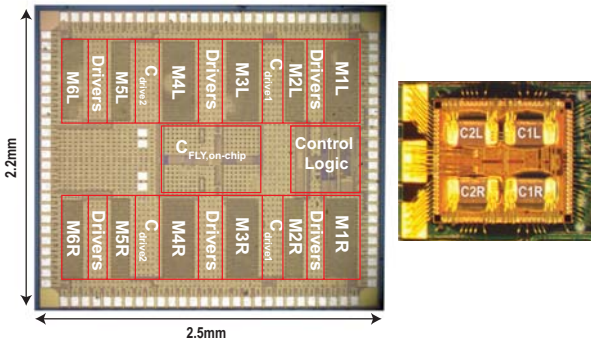

Fig. 6. A die photo and the converter assembly showing the four flying capacitors mounted on top of the chip (5mm^2 220nH inductor is on the back).

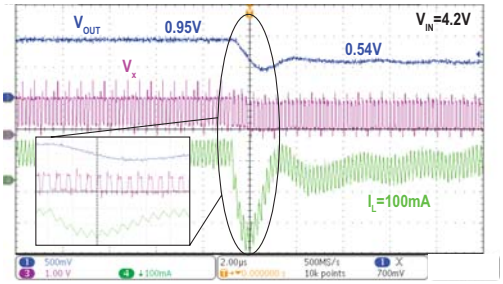

Fig. 7. Measured waveforms of the converter during a Vref step response change.

B. Control Signal Generation

A block diagram of the control logic used to generate the level-shifted control signals for all the drivers, generated from a single PWM signal, is shown in Fig. 4. A one-bit counter is used to toggle the PWM signal between the left and right switches through a phase control signal (Ph_Ctrl). Two level shifters are used to shift the control signals for the two topmost power MOSFETs to boosted voltage levels. Importantly, all the level shifters are powered from the internal rails of the converter ($0.67V_{IN}$ or $0.33V_{IN}$). Deadtime is applied to all the control signals to eliminate short circuit current and to mitigate the internal charge sharing losses between the flying capacitors as indicated previously. A timing diagram of the generated control signals is shown in Fig. 5.

IV. Measurement Results

The converter was implemented in a 180nm CMOS process and wire bonded directly to an interposer. A die photo of the PMIC is shown in Fig. 6. Four 1μF 0.5mm^2 capacitors were mounted on top of the chip and wirebonded directly to the chip pads, while a 5mm^2 220nH inductor and a 1μF 0.5mm^2 were assembled on the bottom side of the interposer. The converter operates at input voltages ranging from 3-to-4.5V and produces output voltages between 0.3-1.2V and a maximum load current of 2.5A at 1V, for a maximum power density of 0.45W/mm^2.

Measurements during transient tests in Fig. 7 reveal that node V_X switches with an amplitude of approximately 1.2V as measured through a resistive debugging trace, indicating correct operation of the internal rail generation. As also shown in Fig. 7, the converter responds in approximately 1.5us during a reference step transient.

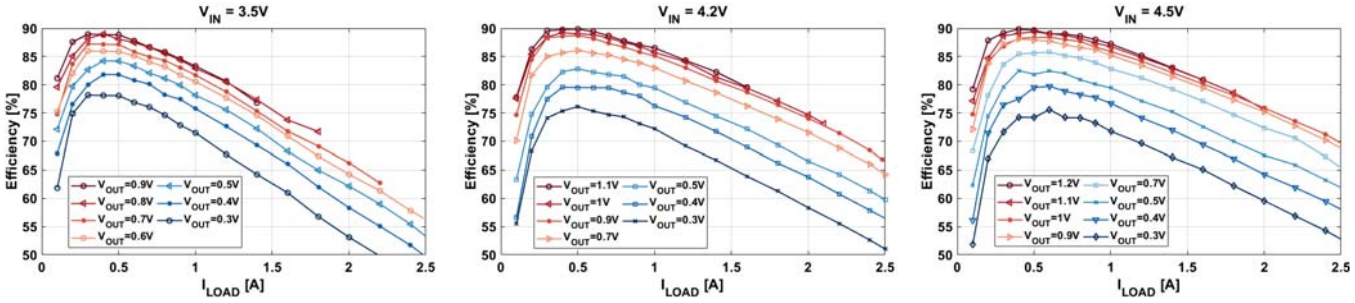

Fig. 8. Measured efficiency versus the load current at different input and output voltages.

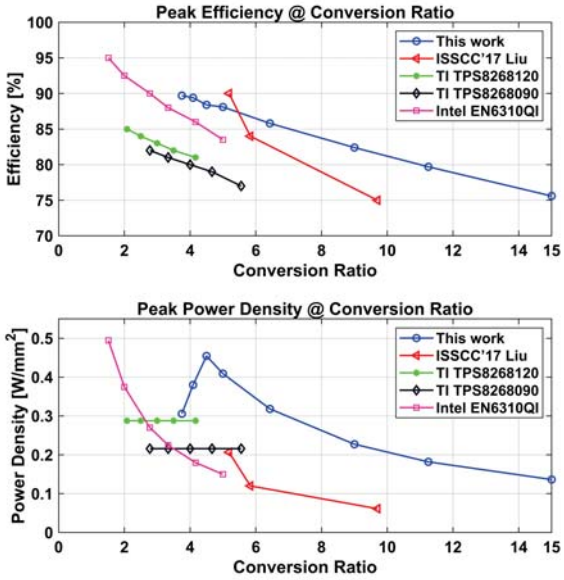

Fig. 9. Measured peak efficiency and peak power density at various conversion ratios.

Measured efficiency results across various input and output voltages are shown in Fig. 8, indicating a peak efficiency of 90% at a power density of 0.11W/mm^2, and an efficiency of 70% at the maximum power density point. Figure 9 shows the peak efficiency and the peak power density at different conversion ratios for this work and previous work including some Li-ion compatible commercial parts, which shows that the proposed converter can maintain mostly higher efficiency and power density compared to prior art for conversion ratios up to 15. Compared to the prior-art Li-ion-compatible converters shown in Table I, the proposed design achieves the highest power density, with higher efficiency, all while supporting high conversion ratios.

V. Conclusion

This paper has presented a DC-DC converter that achieves high power density and efficiency while supporting Li-ion battery voltages via the symmetric modified multilevel ladder topology that reduces the voltage swing on the inductor while topologically supporting low output resistance for low conduction losses. A 180nm implementation operated over conversion ratios from 4 to 15×, and achieved a peak power density of 0.45W/mm^2 and a peak efficiency of 90%.

TABLE I. Table of Comparison to Prior-Art

	TI TPS8268090	TI TPS8268120	ISSCC'17 Liu	CICC'18 Li	This Work
Structure	Buck	Buck	Hybrid (Multilevel Dickon)	Hybrid (Stcked resonant)	Hybrid (SMML)
Process	NR	NR	65nm	150nm	180nm
Input Voltage [V]	2.3 - 5.5	2.3 - 5.5	3.0 – 4.5	3.2 – 4.2	3.0 – 4.5
Output Voltage [V]	0.9	1.2	0.3 – 1.0	0.8 – 1.5	0.3 – 1.2
Peak Output Current [A]	1.6	1.6	1.53	1.5	2.5
Total Area [mm²]	6.67	6.67	6†	14.4	5.5
External rails for drivers?	N/A	N/A	YES ($0.5V_{IN}$)	No	NO
Peak Power Density [W/mm²] @ conv. ratio	0.22†† @ 5.6	0.29†† @ 4.2	0.22†,†† @ 5.2	0.11 @ 3.5	0.45 @ 4.5
Efficiency @ Peak Power Density	65%††	72%††	64%†,††	83.4%	70%
Peak Efficiency (PE) @ conv. ratio	82%†† @ 2.8	85%†† @ 2.1	90%†,†† @ 5.2	87.2% @ 3.2	90% @ 3.8
Power Density [W/mm²] @ PE	0.020††	0.023††	0.04†,††	0.083	0.11
Efficiency @ max. conv. ratio	65%†† @ 5.6	72%†† @ 4.2	75% @ 9.7	70%†† @ 4.5	75.6% @ 15

† Using a 180nH inductor; other measurements mentioned in the paper utilized a 470nH inductor of unspecified size
†† Estimated from plotted data
NR – Not Reported

Acknowledgments

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