8.2 A Continuous-Input-Current Passive-Stacked Third-Order Buck Converter Achieving 0.7W/mm² Power Density and 94% Peak Efficiency

Abdullah Abdulslam, Patrick P. Mercier

University of California, San Diego, La Jolla, CA

The power density and efficiency of power-management integrated circuits (PMICs) is playing an increasingly important role in the miniaturization of modern computing platforms. Small inductors can be used to help miniaturize buck DC-DC converters, however as noted in Fig. 8.2.1 (lower left), small inductors tend to have high DC resistance (DCR) – greater than a comparably-sized CMOS switch – such that they ultimately limit the achievable power density of miniaturized buck converters to <0.4W/mm² when including the area of both the passives and the PMIC [1,2]. While recent work in switched-capacitor (SC) converters has shown that high power density is achievable, it is only possible when employing exotic ultra-high-density capacitors and when operating over a small number of conversion ratios; increasing the number of ratios to support the needs of dynamic voltage scaling loads (e.g., 0.4 to 1.2V) alongside use of conventional capacitor technologies degrades power density to <<0.1W/mm² [3]. Hybrid converters, which process power with both capacitors and inductors, offer an attractive means to potentially increase power density and/or efficiency. Resonating an SC circuit with an inductor can, for example, dramatically increase power density to 0.9W/mm² in [4], however with limited, though improved in [4], ability to regulate beyond the nominal SC ratio at high efficiency. Hybrid multilevel converters can regulate to arbitrary output voltages, though still achieve power density <0.3W/mm² [5], in part due to the increased number of passives and associated higher routing complexity, and in part due to the large conversion ratio in the design in [5].

To further improve power density while supporting regulation of arbitrary output voltages, this paper presents a hybrid DC-DC converter topology, shown in Fig. 8.2.1, that splits the inductor from a conventional buck converter into two half-sized inductors that are stacked on top of and below the input coupling capacitor, which is now flying, to form a passive-stacked 3rd-order buck (PS3B) converter. Unlike the conventional buck converter where the small inductor, which has a larger DCR than the switches in a well-designed comparably-sized PMIC, processes power on the high-current/low-voltage side of the converter, the stacked inductors in the PS3B process power on the low-current/high-voltage side of the converter. Even when accounting for the larger DCR imposed by the half-sized inductors, the overall conduction loss of the PS3B converter is up to 1.4× lower than an equivalent-area conventional buck converter. The input current in the PS3B is also continuous, in stark contrast to the fully pulsated input current of a conventional buck converter, which helps reduce the area of the passives required for filtering. Compared to a 2-phase buck converter, the PS3B has the same theoretical conduction losses at D=0.5, though, importantly, with fewer power transistors (2 vs. 4) and fewer power pins (3 vs. 4), which facilitates less routing complexity that, when combined with the lack of area and/or energy-consuming inter-phase alignment circuits (e.g., series current sensing resistors or equivalent), enables an overall increase in power density compared to prior-art when including the area of the passives [6].

Figure 8.2.2 shows a detailed circuit diagram of the converter along with its operating principle. In phase $Ø_1$, V_{OUT} is connected to V_{X1} via M_1, and thus L_1 experiences a positive voltage of (V_{IN}-V_{OUT}) and is energized, L_2 experiences a negative voltage (V_{OUT}-V_{IN}) and is deenergized, while C_F discharges to the output via I_2. In phase $Ø_2$, V_{OUT} is connected to V_{X2} via M_2, and thus L_2 experience a positive voltage (V_{OUT}) and is energized, L_1 experience a negative voltage (-V_{OUT}) and is deenergized, and C_F is charged via I_1. Thus, V_{X1} switches between V_{OUT} and (V_{OUT}+V_{IN}), while V_{X2} switches between (V_{OUT}-V_{IN}) and V_{OUT}. Accordingly, based on inductor volt-second balance, the voltage on C_F is balanced at V_{IN} while V_{OUT}=DV_{IN}, which is exactly the same relationship as a conventional buck converter, though in this case via three reactive elements – hence it is a 3rd-order buck.

Since V_{X1} and V_{X2} switch between non-standard voltages, M_1 and M_2 are driven with level-shifted signals generated via on-chip MOS-based bootstrapping capacitors, C_{boot1} and C_{boot2}. Here, the top plate of C_{boot1} is nominally charged to (V_{OUT}+V_{IN}) during phase $Ø_2$ via M_{13}, while the bottom plate of C_{boot2} is nominally charged to (V_{OUT}-V_{IN}) during phase $Ø_1$ via M_{23}, with the other terminals of both capacitors connected to V_{OUT} at all times. A deadtime circuit is used to avoid short-circuit current by transitioning from $Ø_1$ to $Ø_2$ according to the following sequence: 1) C_{boot1} is disconnected from M_1 as M_{12} turns off, and the gate capacitance of M_1 is discharged to V_{OUT} since M_{11} turns on; 2) C_{boot2} is disconnected from V_{X2} as M_{23} turns off; 3) C_{boot2} discharges the gate capacitance of M_2 to (V_{OUT}-V_{IN}) as M_{22} turns on; and 4) C_{boot1} is connected to V_{X1} for its top plate to be charged to (V_{OUT}+V_{IN}). Transitioning from $Ø_2$ to $Ø_1$ is done through the reverse manner. Although the voltages at V_{X1} and V_{X2} operate over V_{IN} or below ground, all of the MOSFETs, the bootstrapping capacitors, and the flying capacitor only ever experience a blocking voltage of V_{IN}, thereby ensuring reliable operation. Importantly, the parasitics of the power MOSFETs experience the same ΔV as a conventional buck, and thus do not suffer from additional switching losses. To mitigate potential ringing on the MOSFET driver lines from bondwire inductance, a small on-chip MIM capacitor, $C_{F,on\text{-}chip}$, is placed in parallel to the off-chip C_F.

Figure 8.2.3 shows the controller used to generate the four control signals of the converter. Two-stage level-shifters shift the control signals from {0,V_{IN}} to the appropriate levels for the drivers. All of the drivers and the level shifters are powered by either V_{OUT} or by one of the two bootstrapping capacitors, and thus no external voltage sources are needed. The timing between the different control signals is adjusted carefully through a deadtime circuit so that the dis/charging of MOSFETs' gate capacitance and the bootstrapping capacitors is done in the proper sequence. As shown in Fig. 8.2.3, C_{boot2} is implemented in deep *n*-well since its bottom-plate experiences a negative voltage, while C_{boot1} is implemented as a usual MOS capacitor. Interestingly, the bulk of the chip is biased at V_{OUT} instead of ground for convenience, since the power MOSFETs and most of the driver switches are referenced to V_{OUT} (though through use of deep *n*-wells this is not strictly necessary).

The PS3B converter is implemented in a 1.85mm² 0.18µm CMOS chip, which is wirebonded to a 5mm² interposer comprising two 1.3mm² 240nH inductors (L_1 and L_2), two 0.5mm² 470nF capacitors (C_F and C_{OUT}), and all necessary routing and wirebonds as shown in Fig. 8.2.3. The converter operates with V_{IN}=1.8V, which is a rail commonly found in mobile, desktop, and server-grade computing platforms, and generates SoC-compatible voltages between 0.4 and 1.5V at currents up to 2.5A. Since the input current is continuous, no additional input capacitors are needed, saving additional area compared to conventional implementations. Measurement results in Fig. 8.2.4 show that V_{X1} and V_{X2} switch as expected at up to 6.5MHz to generate V_{OUT}, and under PWM control the converter has <50mA input current ripple, <20mV output voltage ripple, and can respond to a 0-to-1A current step with <170mV droop in <20µs. The converter achieves a peak power density of 0.7W/mm² at an efficiency of 86.6%, and a peak efficiency of 94% at a power density of 0.18W/mm², with both figures including the full area of the converter, passives, and wirebonding/routing. If considering only the area of the passives, assuming advanced packaging is available to reduce interconnect area, then the converter achieves a power density of 1W/mm². Compared to prior art summarized in Figs. 8.2.5 and 8.2.6, the converter achieves >2× higher power density or 16% higher efficiency amongst designs that efficiently operate across a wide, SoC-compatible voltage range, and that report the size of the passives. A photograph of the assembled PMIC is shown in Fig. 8.2.7.

Acknowledgements:
This work was supported by pSemi Corporation.

References:

[1] S. J. Kim et al., "High Frequency Buck Converter Design Using Time-Based Control Techniques," *IEEE JSSC,* vol. 50, no. 4, pp. 990-1001, 2015.

[2] Texas Instruments, TPS8268150 Data sheet Rev C., "TPS8268x 1600-mA High-Efficiency MicroSiP™ Step-Down Converter Module," Oct. 2014, Revised June 2015, Accessed Oct. 2018, <www.ti.com/lit/gpn/tps8268150>.

[3] Y. Jiang et al., "A 0.22-to-2.4V-Input Fine-Grained Fully Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Achieving 84.1% Peak Efficiency at 13.2mW/mm²," *ISSCC,* pp. 422-424, Feb. 2018.

[4] C. Schaef et al., "A Variable-Conversion-Ratio 3-Phase Resonant Switched Capacitor Converter with 85% Efficiency at 0.91W/mm² Using 1.1nH PCB-Trace Inductors," *ISSCC,* pp. 1-3, Feb. 2015.

[5] W. Liu et al., "A 94.2%-Peak-Efficiency 1.53A Direct-Battery-Hook-Up Hybrid Dickson Switched-Capacitor DC-DC Converter with Wide Continuous Conversion Ratio in 65nm CMOS," *ISSCC,* pp. 182-183, Feb. 2017.

[6] B. Lee et al., "A 25MHz 4-Phase SAW Hysteretic DC-DC Converter with 1-Cycle APC Achieving 190ns T_{settle} to 4A Load Transient and Above 80% Efficiency in 96.7% of the Power Range," *ISSCC*, pp. 190-191, Feb. 2017.

 978-1-5386-8531-0/19/$31.00

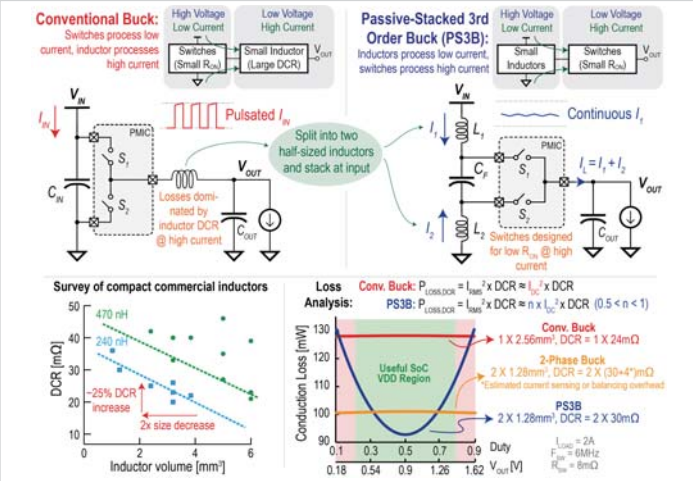

Figure 8.2.1: A conventional buck converter (top left) vs. the PS3B converter (top right) designed to operate small inductors, which have high DCR (bottom left), at the high-voltage low-current side of the converter to minimize conduction losses (bottom right).

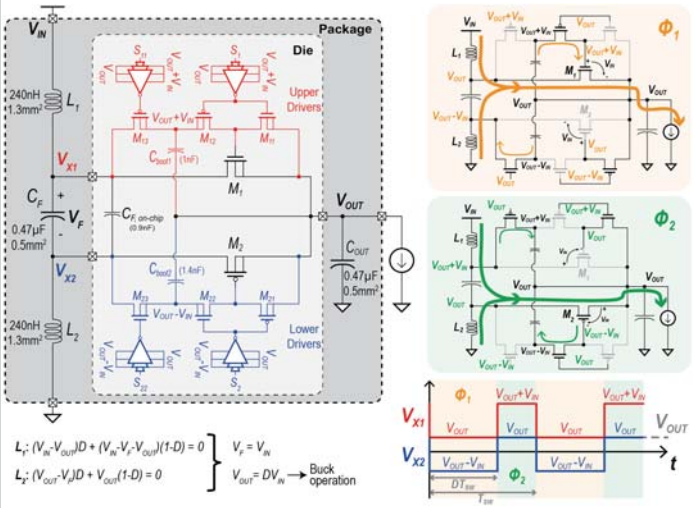

Figure 8.2.2: Schematic of the PS3B converter, along with associated timing diagrams.

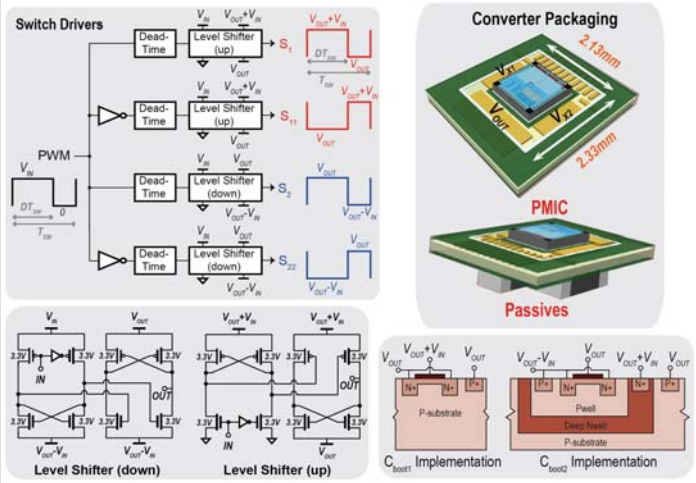

Figure 8.2.3: Generation of level-shifted signals from an input PWM signal (top left); level-shifter schematics (bottom left); 3D render of converter packaging (top right); bootstrap capacitor cross-section (bottom right).

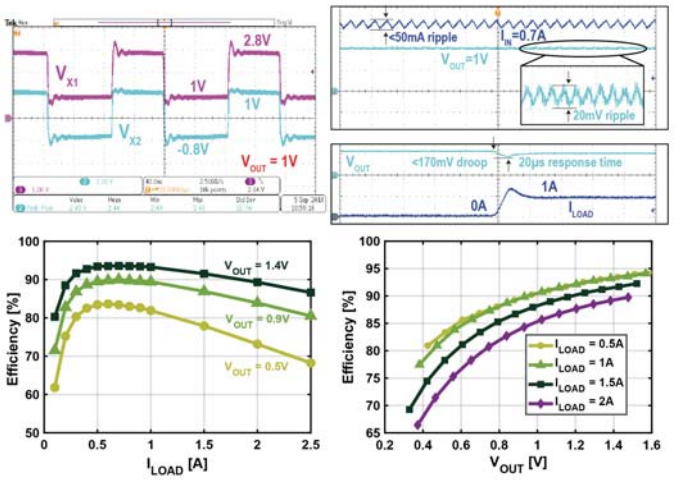

Figure 8.2.4: Measured internal waveforms of the converter (top left); measured input current ripple, output voltage ripple, and response time during a 0-to-1A load step (top right); efficiency vs. load current (bottom left) and output voltage (bottom right).

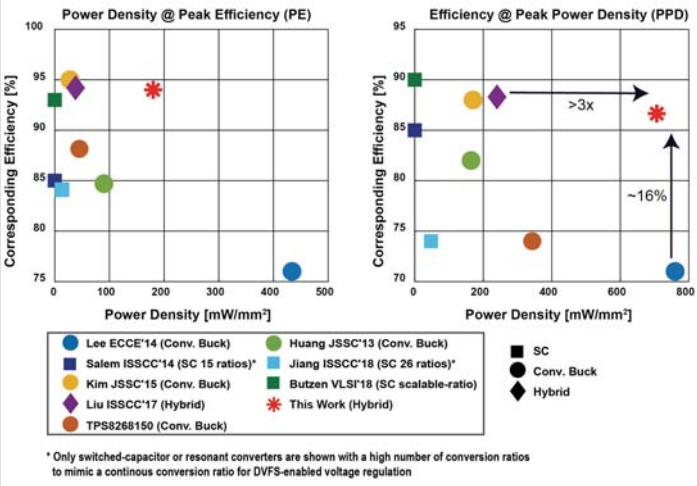

Figure 8.2.5: Measured efficiency and power density compared to prior-art converters that can efficiently regulate across SoC-compatible voltages and that report the total converter area (including the area of the passives and the interconnection between them).

	Kim JSSC'15	Lee ISSCC'17	Liu ISSCC'17	Jia JSSC'18	Jiang ISSCC'18	TI TPS8268150	This Work
Topology	Buck	Buck (4-phase)	Hybrid (Multilevel)	Buck	SC (26 ratios)	Buck	Hybrid (PS3B)
Technology	65nm	350nm	65nm	65nm	65nm	NR	180nm
Input Voltage [V]	1.8	3.3	3.0 – 4.5	1.1	0.22 – 2.4	2.3 - 5.5	1.8
Output Voltage [V]	0.6 – 1.5	0.3 – 2.5	0.3 – 1.0	0.3 – 0.86	0.85 – 1.2	1.5	0.5 – 1.5
I_{LOAD} (MAX) [A]	0.6	6	1.53	0.04	0.08	1.6	2.5
Input Current	Pulsated	Pulsated	Pulsated	Pulsated	Pulsated	Pulsated	Continuous
PMIC Area [mm²]	5	1.88	4.05	0.13	2.42	6.67	1.85
Total Footprint [mm²]	5	NR	6**	0.13	2.42	6.67	5
Peak Efficiency (PE)	95.5%	88.1%	94.2%	73%	84.1%	88%***	94%
Power Density @ PE * [W/mm²]	0.03***	NR****	0.04**	NR	0.013	0.045***	0.18 (0.25**)
Peak Power Density (PPD) * [W/mm²]	0.17	NR****	0.24	0.27	0.034***	0.36***	0.7 (1.0**)
Efficiency @ PPD	88%	NR****	88.3%	NR	74%***	74%***	86.6%

NR – Not Reported
* Unless otherwise specified, power densities are computed with respect to the total converter footprint including the passives and routing
** Computed by summing the area of the passive component footprints
*** Estimated from measurement results
**** The area of the passives are not reported

Figure 8.2.6: Comparison to prior-art converters that operate across SoC-compatible voltage ranges.

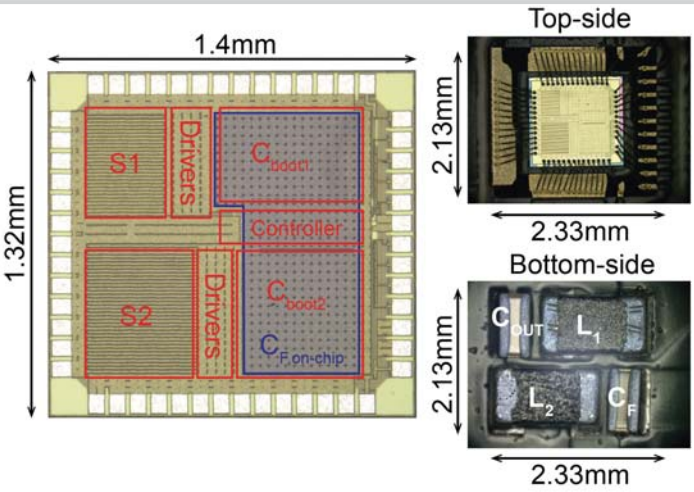

Figure 8.2.7: Micrograph of the fabricated stacked-passives 3rd-order buck converter (left); top side of the wirebonded prototype (top right); bottom side of the prototype (bottom right). The converter occupies 5mm² including the PMIC, passives, and the package area including the wirebonds and pads.

978-1-5386-8531-0/19/$31.00