15 GHz 25 dBm Multigate-Cell Stacked CMOS Power Amplifier with 32 % PAE and $\geq$ 30 dB Gain for 5G Applications

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***Abstract*—A three-stage stacked FET CMOS power amplifier (PA) for the 12.7 to 15.3 GHz frequency range is presented. The PA achieves more than 30 dB linear gain with saturated output power of 25.1 dBm (320 mW) and peak power added efficiency (PAE) of 32.4 % at 13.5 GHz. The PA is implemented in 45 nm CMOS SOI technology. High gain is achieved with two cascode pre-driver stages and a final high power stage. The output stage comprises 512 four-stack multigate-cell devices to allow high voltage swings and correspondingly high output power. The effective gate width of the output device is $614\,\mu$m. To the authors knowledge, combination of power and efficiency achieved in this work are the highest reported for CMOS PAs in the 15 GHz band. The amplifier occupies an area of $1 \times 1\,\mathrm{mm}^2$ including pads.**

***Index Terms*—CMOS, power amplifier (PA), millimeter-wave integrated circuits, stacked power amplifier, 15 GHz band, 5G transmitters.**

I. Introduction

Next generation 5G communication systems are expected to provide significantly higher data rates and reduced latency by utilizing various techniques, which include the use of higher carrier frequencies ranging from 6 to 100 GHz, larger modulation bandwidths and large numbers of antennas per transmitter. Active research for 5G systems is being conducted at frequency bands including the 15 GHz [1], 28 GHz, 60 GHz, and 70 GHz bands.

In a massive MIMO transmitter, the power level required for each antenna element varies inversely with the number of antennas. It is estimated that peak power levels needed to drive antennas for base-stations at 15 GHz are in the range of 20 to 27 dBm. Other features important for PAs include high efficiency, linearity, ability to be co-integrated with other RF front-end circuits, and low cost. In this paper, we report a CMOS PA with promising characteristics for 5G applications at 15 GHz. CMOS is a major contender as a result of the modest power levels needed, the potential for low cost fabrication, as well as the ability to be integrated with switches, LNAs, mixers, and digital control circuitry.

Traditionally, the output power levels that could be produced with a CMOS PA were limited due to the small voltage handling capability of FETs. Recent research has shown that the limited CMOS voltage handling capability, and thus the obtainable power levels, can be substantially increased by means of FET transistor stacking (series connection.) It has been shown that with appropriate biasing and loading a uniform voltage swing distribution can be achieved on all of the series devices, such that the overall voltage swing can reach $N \times \mathrm{V_{max}}$, where N is the number of series transistors, and $\mathrm{V_{max}}$ is the maximum voltage allowed on a single FET for reliable operation [2]. In [3], a compact unit cell was proposed in 45nm CMOS SOI technology that implements a 4-stack multigate device. The multigate-cell significantly reduces the parasitic interconnections between the stacked transistors and provides controllable capacitance at the gates of each stacked FET.

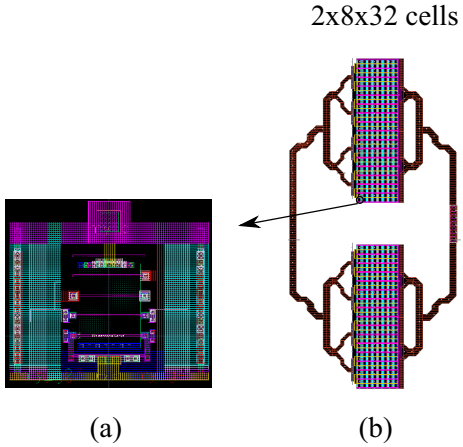

Fig. 1. (a) Layout of a single NFET multigate-cell, (b) the final stage 2x256 cell device.

In this work, the concept of the 4-stack multigate-cell has been used to implement a high output power and high gain tuned PA in the 15 GHz band. The PA consists of three stages and includes both input and output matching networks. The peak realized gain is more than 30 dB at 13.5 GHz with $\geq$ 25 dBm saturated output power and 32.4 % peak PAE. To the authors' knowledge, the combination of power and efficiency achieved in this work are the highest reported for CMOS PAs in the 15 GHz band.

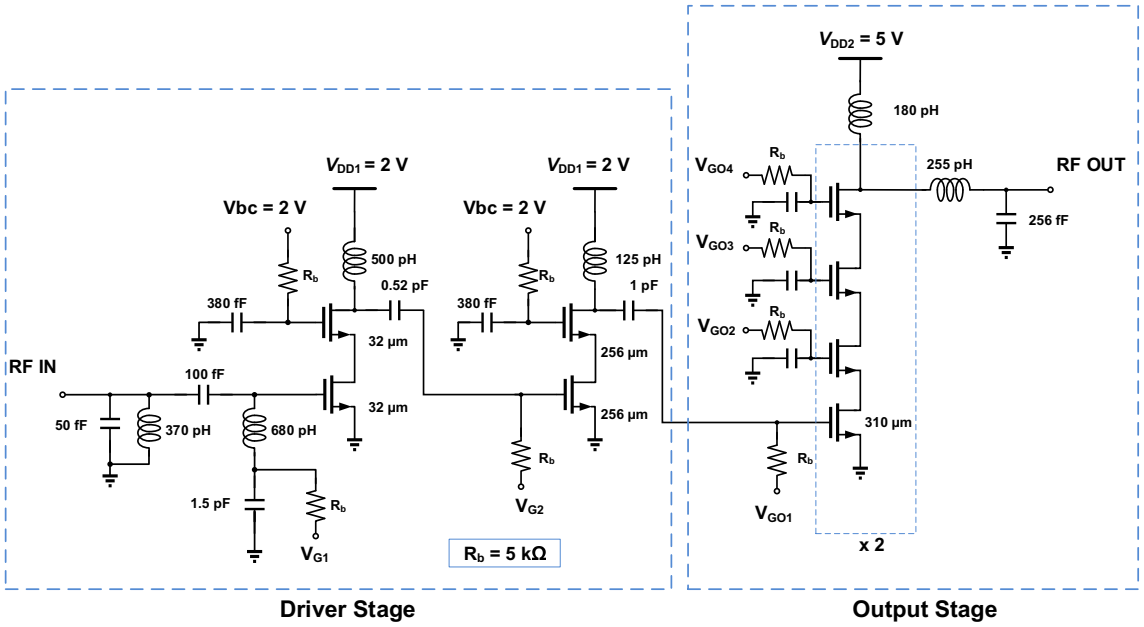

Fig. 2. The circuit schematic of the three stage multigate-cell stacked CMOS power amplifier.

II. Circuit Architecture and Design

As mentioned, in a CMOS process, high output power can be achieved by stacking multiple transistors in series. In this work, we use the multigate FET unit cells, each of which comprises a stack of four NMOS transistors [3]. The unit cell is implemented as a single FET device with four fingers of $\mathrm{w_g}$ width. The contacts to intermediate source and drain nodes are eliminated, resulting in a significant reduction of parasitic capacitances and resistances. Each of the four gates in a unit cell is separately connected to a different gate capacitor. These are Metal-Oxide-Metal (MOM) capacitors which are constructed around the transistor using various metalization layers. The top view of the layout of the multigate-cell is depicted in Fig. 1a. A detailed description of the multigate-cell can be found in [3].

The multigate-cells can be arranged in an array of M elements to form an overall device width of $M \times \mathrm{w_g}$. Thus, a compact stacked FET power amplifier design can be realized based on combinations of the unit cell. The number of elements M is constrained, however, due to the difficulty of ensuring phase coherence between cells spaced far apart.

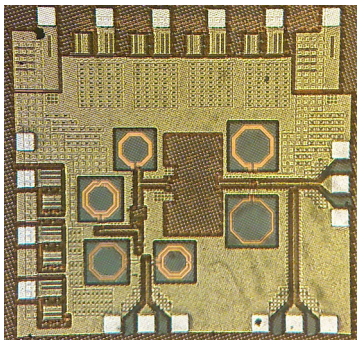

Fig. 3. Micrograph of the $1\mathrm{x}1\,\mathrm{mm}^2$, three stage power amplifier chip.

The circuit diagram of the complete 15 GHz power amplifier is shown in Fig. 2. The PA contains a two stage cascode pre-driver and a high power 4-stack multigate-cell output stage. The pre-driver stages, together with the output stage, realize more than 30 dB gain. Such high gain facilitates the full integration of the PA into a CMOS transmitter IC.

The output stage contains an array of two 8 x 32 unit cells with a single cell width of $\mathrm{w_g} = 1.2\mu m$ was used to achieve $2 \times 256 \times 1.2\,\mu\mathrm{m} = 614\,\mu\mathrm{m}$ total width. Thin oxide minimum length devices were used in each cell. The top view of the output device layout shown in Fig. 1b. Because of the large voltage swing handling capability of the 4-stack, the optimum load impedance of the output stage is approximately $20\,\Omega$, allowing simple low Q matching to $50\,\Omega$. Simple first order matching networks with on chip inductors were used both in the input and the output as well as in the inter-stage matching networks.

The multigate-cell PA was fabricated in the IBM 45 nm SOI CMOS process. The PA occupies a compact chip area of $1\,\mathrm{mm}^2$ including pads. The chip micrograph is shown in Fig. 3. The chip also contains a -30 dB output coupler for monitoring the output signal to enable predistortion.

III. Measurement Results

Because of the large gain, the bias points of pre-driver stages were restricted in order to maintain unconditional stability. Supply voltages of the pre-driver stages were fixed at $\mathrm{V_{DD1}} = 2\,\mathrm{V}$ and of the final stage at $\mathrm{V_{DD2}} = 5\,\mathrm{V}$. Fig. 4 shows measured small-signal S-parameters and the stability

TABLE I
SUMMARY OF THE PERFORMANCE OF THE CMOS POWER AMPLIFIERS

Ref.	Technology	Freq. (GHz)	Psat (dBm)	Peak PAE (%)	Gain (dB)	Design	VDD (V)	Chip Area (mm^2)
[4]	45 nm SOI CMOS	10 - 35 @ 18 GHz	27	11.8	5	8-Stack	9.6	0.33
[5]	45 nm SOI CMOS	4 - 50 @ 15 GHz	22.5	24.2	22	3-Stack Differential	6.6	0.28
[6]	90 nm CMOS	5.2 - 13 @ 8 GHz	25.2	21.6	19	Differential Push-Pull	2.8	0.7
[7]	180 nm CMOS	7 - 12 @ 10 GHz	23.8	25.8	14.5	Two Cascode Combined	3.6	0.47
[8]	110 nm CMOS	6.5 - 15 @ 9 GHz	20.3	28.9	11.6	1 Stage Cascode	2.6	0.7
[9]	0.25um SiGe BiCMOS	12 - 16 @ 14 GHz	24.45	29.1	15.5	1 Stage Cascode	4	0.384
This work	**45 nm SOI CMOS**	**12 - 15 @ 13.5 GHz**	**25.1**	**32.4**	**30**	**2 cascode drivers, 4-stack final stage**	**5**	**1**

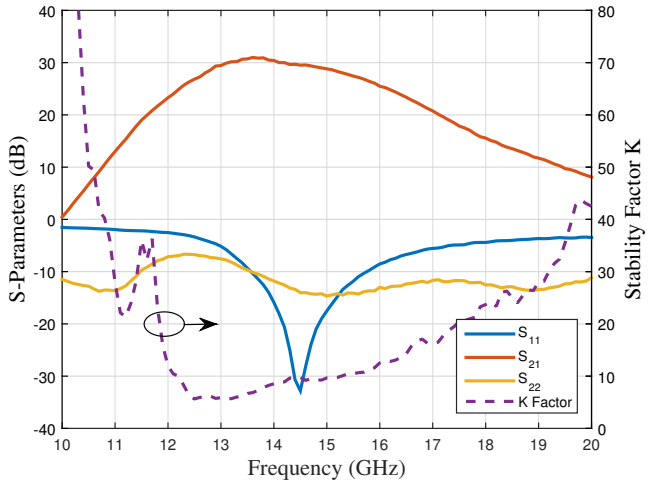

Fig. 4. Amplifier s-parameters for $V_{G1} = 0.5\,V$, $V_{G2} = 0.3\,V$, and $V_{GO2} = 0.45\,V$.

factor K of the PA from 10 to 20 GHz when biased in a stable operation mode with $V_{G1} = 0.5\,V$, $V_{G2} = 0.3\,V$, and $V_{GO2} = 0.45\,V$. Under these biasing conditions, the PA is unconditionally stable ($K > 5.6$). The PA demonstrates a peak S_{21} gain of 31 dB at 13.5 GHz with a -3 dB bandwidth from 12.7 to 15.3 GHz, which results in a fractional bandwidth of 20 %. Both the input and the output reflection coefficients lie below -10 dB in the 13.5 to 15.5 GHz frequency band.

Fig. 5 illustrates the measured large signal gain, power added efficiency (PAE), and the drain efficiency η_D of the final stage at 13.5 GHz under stable biasing conditions. Both class A ($V_{GO1} = 0.45\,V$) and class AB ($V_{GO1} = 0.3\,V$) modes of operation of the final stage are shown (gate voltages of the stack transistors were changed accordingly.) The PA achieves maximum saturated output power $P_{sat} = 25.1\,dBm\,(323.5\,mW)$. The peak PAE and drain efficiency are 32.4 % and 36.4 %, respectively. Fig. 6 shows values of P_{sat} over the frequency.

Table I gives an overview of the currently reported CMOS power amplifiers in the X-band or in the Ku-band. The performance of the multigate-cell CMOS power amplifier presented in this work features both high power and high efficiency, and provides the best combination of saturated output power and efficiency reported to date. Power levels of the same order were also reported for the SiGe BiCMOS process [10]. Higher output power was demonstrated at 15 GHz by an 8 FET CMOS stack circuit, although the efficiency reported was relatively low.

IV. CONCLUSION

A three stage, 4-stack FET CMOS power amplifier has been presented. The design of the amplifier uses 512 multigate-cells to form a 4-stack output device with 614 μm effective gate

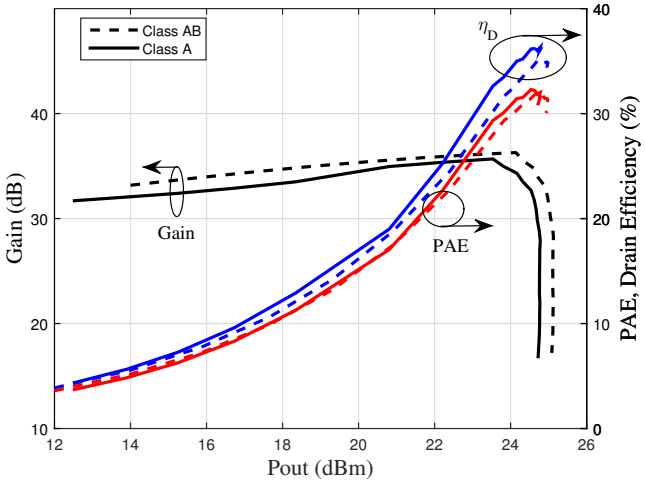

Fig. 5. Amplifier Gain, PAE and drain efficiency η_D vs. output power at 13.5 GHz for $V_{G1} = 0.5\,V$, $V_{G2} = 0.3\,V$, and final stage in class A ($V_{GO2} = 0.45\,V$) or Class AB ($V_{GO2} = 0.3\,V$.)

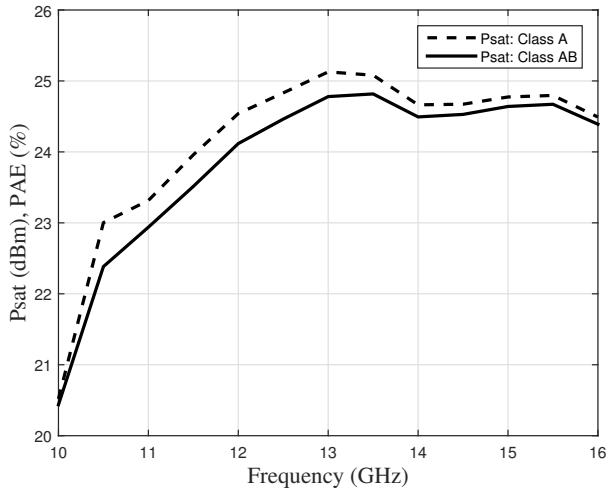

Fig. 6. Amplifier saturated output power $\mathrm{P_{sat}}$ vs. frequency for $\mathrm{V_{G1}} = 0.5\,\mathrm{V}$, $\mathrm{V_{G2}} = 0.3\,\mathrm{V}$, and final stage in class A ($\mathrm{V_{GO2}} = 0.45\,\mathrm{V}$) or Class AB ($\mathrm{V_{GO2}} = 0.3\,\mathrm{V}$.)

width. The high power output stage, together with the two stage cascode pre-drivers achieve more than 30 dB linear gain centered around 13.5 GHz. The small-signal -3 dB bandwidth is 2.6 GHz (20%). The amplifier achieves output power of more than 323 mW and a peak PAE of 32.4 % at 13.5 GHz.

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